Docket No.: 64965-134 PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Jeffrey DWORK	:	Confirmation Number: 5785
Serial No.: 09/505,062	:	Group Art Unit: 2665
Filed: February 16, 2000	:	Examiner: Thien D. Tran

For: METHOD AND APPARATUS FOR AUTOPOLLING PHYSICAL LAYER DEVICES IN A NETWORK

TRANSMITTAL OF APPEAL BRIEF

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Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed . Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

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Sir:

This Brief is submitted pursuant to the appeal of the final rejection of claims 1-9 and 11-17 filed December 11, 2003.

I. REAL PARTY IN INTEREST

The real party in interest in this Application is the Assignee, Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences believed to affect or be affected by a decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-9 and 11-17 stand under final rejection. Claims 10, 18 and 19 were objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, these claims have not been amended to be in independent form at this time.

IV. STATUS OF AMENDMENTS

No Amendment has been filed after the final rejection.

V. SUMMARY OF INVENTION

The present invention addresses and solves problems related to software overhead in determining network conditions from the information contained in the registers of external physical layer (PHY) devices. This is accomplished through auto-poll registers that contain the register numbers and addresses of the PHY registers that will be polled. The auto-poll logic examines the auto-poll registers to determine whether auto-polling is enabled for a particular register. When changes are detected from the results of previous polling, an attempt is generated to inform the host CPU that the network conditions have changed. Software overhead to determine these network conditions is thereby avoided through the automatic polling logic and registers.

Referring to Fig. 3 and pages 5-8 of the present Application, the auto-polling logic and associated auto-polling registers will be described. The auto-poll logic 70 implements the automatic polling function of the present invention. The auto-poll logic 70 operates in conjunction with poll registers 72 and poll data registers 74. In certain embodiments, there is a 1-to-1 correspondence between the number of poll registers 72 and poll data registers 74.

The automatic polling of the PHY registers 76 contained in each of the PHY devices 62 is controlled by the information contained in the six poll registers 72. By writing to one of the poll registers 72, a user independently defines the PHY addresses and register numbers for external PHY registers 76. As apparent from the block diagram of Fig. 3, the external PHY registers 76 are not restricted to a single PHY device 62.

Referring now to page 6, the various fields contained in a typical poll register 72 are described. For purposes of this Appeal, bits 12-8 and 4-0 are of most relevance. Bits 12-8 form the field that contains the register number of an external PHY register that the auto-poll state machine will periodically read, assuming the auto polling function is enabled. Bits 4-0 form the field that contains the address of the external PHY that contains the external PHY register that will be periodically read. In other words, one of the fields contains the address of the external PHY device 62, and the other field contains the address of a specific PHY register 76 within the specified PHY device 62. Hence, as depicted in Fig. 3, a single PHY device may contain a number of different PHY registers 76, for example six in Fig. 3. The poll register 72 of the present invention allows poll logic 70 to automatically poll a specified one of the PHY registers 76. This produces a level of granularity in the auto polling that is finer than merely a selection of the PHY device 62.

VI. ISSUES

1. Whether claims 1-9 and 11-17 stand properly rejected under 35 U.S.C. § 102(e) as anticipated by Booth (U.S. Patent No. 6,065,073).

VII. GROUPING OF CLAIMS

As to the grounds of rejection of claims 1-9 and 11-17, the rejected claims do not stand or fall together as a single group. Claims 1-4 stand or fall together as a group. Claims 5-9 each stand alone

and will be separately argued. Claims 11-12 stand or fall together as a group. Claims 13 and 16-19 each stand alone and will be argued separately. Claim 14 and 15 stand or fall together as a group.

VIII. REJECTIONS

Claims 1-9 and 11-17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Booth.

IX. THE REFERENCE

Booth discloses an auto polling unit for interrupt generation in a network interface device and depicts the auto polling unit 920 in Fig. 11. The description of the auto polling unit 920 is provided in columns 19 and 20.

The auto polling unit 920 includes a host CPU data register 914, an auto poll data register 916A, an auto poll hold data register 916B, an auto poll control unit 919, an interrupt status data multiplexer 922, and a comparator 912. The operation of the auto polling unit 920 is governed according to an auto polling state machine described in Fig. 12.

When the host CPU 202 begins writing a PHY, the auto polling unit 920 is able to determine the address of the PHY device that it will eventually poll. Booth does not make clear how the auto polling unit 920 is able to determine the address of the PHY device that it will eventually poll. Referring now to column 20, lines 4-53, the auto-poll read operation involves auto polling unit 920 accessing a status register 944 of a currently selected PHY device via a management interface. The value read from the status register 944 of the currently selected PHY device is conveyed to the auto poll registers 916A-B via management interface logic unit 930. The contents of the auto poll data register 916A are then conveyed to comparator 912, which also receives the contents of host CPU data register 914. After the auto poll read, comparator 912 performs a comparison of the current status value from register 916A and the most recent status value read by the host CPU. If there is a mismatch

detected between the two values, an interrupt to the host CPU is generated. The host CPU responds to the assertion of the interrupt signal by requesting a read of the status register data which caused the interrupt. This data is conveyed to the host CPU from the auto poll hold data register 916B. The read request by the CPU also causes the registers 914 and 916A to update the same value to de-assert the interrupt signal 924. The de-assertion of the interrupt signal causes the state machine to transition to reset the counter time out and return to the monitoring state. In this manner, auto-polling is disabled while interrupt signal 924 is asserted.

X. ARGUMENTS

A. The rejection of claims 1-4 under 35 U.S.C. § 102(e) as anticipated by Booth is improper since Booth fails to identically disclose each and every element of the claimed invention.

Claim 1 requires an arrangement for polling PHY registers in the network, comprising a number of poll registers that store information indicating which PHY registers are to be polled. The arrangement also comprises a number of poll data registers that receive polled information from the PHY registers. The poll logic automatically polls those PHY registers indicated by the information in the poll registers as PHY registers to be polled, and stores the polled information in the PHY registers. Booth fails to disclose poll registers that store information indicating which PHY registers are to be polled.

The Examiner is charged with the initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention under any statutory provision. *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997). Lack of novelty under 35 U.S.C. § 102 requires the **identical** disclosure in a single reference of each element of a claimed invention such as to establish that the

identically claimed invention is in the public domain and that such existence would have been recognized by one having ordinary skill in the art. *Crown Operations International Ltd. v. Solutia, Inc.*, 62 USPQ2d 1917, 1921; *In re Spada*, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); *Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 678, 7 USPQ2d 1315, 1317 (Fed. Cir. 1988). Accordingly, in imposing the rejection under 35 U.S.C. § 102, the Examiner is required to point to "page and line" wherein a single reference identically discloses each feature of the claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993).

The Examiner has failed to point out poll registers that store information indicating which PHY registers are to be polled. As discussed in column 19, lines 57-62 of Booth, when the host CPU 202 begins writing a PHY, auto-polling unit 920 is able to determine the address of the PHY device that eventually will be polled. However, this description does not identically disclose a number of poll registers that store information indicating which PHY registers are to be polled. This passage only describes the ability of an auto-polling unit to somehow determine the address of an entire PHY device that will eventually be polled. Firstly, **the passage does not describe any register in which information is stored indicating which PHY device is to be polled**. Secondly, even if Booth disclosed registers that store information indicating which PHY devices are to be polled, it does not describe poll registers that store information indicating which PHY **registers** are to be polled.

PHY devices may have a number of registers, as depicted in Fig. 3 of the present specification. For example, a single PHY device 62 may contain six different PHY registers 76. Booth fails entirely to show poll registers that store information indicating which PHY registers are to be polled. Since claim 1 of the present invention requires a number of poll registers that store information indicating which PHY registers are to be polled, and Booth fails to identically disclose such a feature, the rejection of claim 1 and those claims dependent therefrom under 35 U.S.C. § 102(e) must fail.

In attempting to buttress his argument that Booth discloses a number of poll registers that store information indicating which PHY registers are to be polled, the Examiner cobbled together certain portions of the disclosure in a manner not supported by the facts of the disclosure. In particular, the Examiner states that unit 920 is able to determine the address of which PHY device is to be polled, referring to column 19, lines 60-67, by comparing the current values or information with the most recent values or information in the auto-polled data registers 916. The Examiner states that if there is a difference in the comparison to one of the particular registers 916, for example 916A, then the corresponding PHY PCS to that particular register 916A being polled in the auto-poll process. Therefore, the Examiner states that "auto-poll data registers 916 are considered as holding information to which the particular PHY PCS module being polled or not." (referring to column 20, lines 15-65). Apparently therefore, the Examiner equates the auto-poll data register 916A and auto-poll hold data register 916B, with the poll registers of the present invention that store information indicating which PHY registers are to be polled. However, neither of the auto-poll registers 916A, 916B store information indicating which PHY registers are to be polled. As can best be determined by a review of Booth, from column 20, lines 15-17, the auto-poll registers 916A-B appear to receive the value read from the status register 944 of the currently selected PHY device. Hence, **neither of the auto-poll registers 916A-B contains information indicating which PHY registers are to be polled**. Instead, they just contain status value information from the status registers 944 of the currently selected PHY devices.

To deny patentability to an inventor under 35 U.S.C. § 102, a reference must identically disclose each and every element of the claimed invention. It is not enough for a reference to nearly disclose or somewhat disclose the invention. The disclosure must be identical to the invention claimed. Under such a rigorous standard, Booth must be seen to fail to disclose each and every

element of the invention. The rejection of claims 1-4 under 35 U.S.C. § 102(e) is therefore flawed and should be overturned.

B. The rejection of claims 5-9 under 35 U.S.C. § 102(e) is improper since Booth does not identically disclose each and every element of these claims.

Claim 5 of the present invention claims that n=m, where the number n is the number of poll registers that store information indicating which PHY registers are to be polled, and the number m is the number of polled data registers that receive polled information from the PHY registers. The Examiner has failed to establish wherein Booth discloses the number of poll registers that store information indicating which PHY registers could be polled. The registers 916A, 916B of Booth receive the polled information from the PHY registers, as described at column 20, lines 15-17. It is improper to ascribe to these very same registers the function of storing information indicating which of the PHY registers are to be polled. There is no support for such an assertion. Therefore, the number n of poll registers that store information indicating which PHY registers are to be polled in Booth is the number zero (0). Both of registers 916A, 916B receive the polled information from the PHY registers, such that the number m is equal to 2. Therefore, m = 2, and n =0, so that $n \neq m$. Booth therefore does **not** satisfy the limitations of claim 5 exactly. Hence, the rejection of this claim under 35 U.S.C. § 102(e) is improper.

Claim 6 describes that each of the poll registers includes an address field that contains an address of a PHY containing a PHY register to be polled. However, the Examiner has failed to establish that Booth discloses poll registers whatsoever. The Examiner refers to column 5, lines 45-65. This reference refers to the prior art and not to any poll registers alleged by the Examiner to be present in the Booth embodiment described in Fig. 11. Further, the suited portion of Booth does not describe

an address field that contains an address of a PHY containing a PHY register to be polled. Therefore, claim 6 is not identically disclosed in Booth.

Claim 7 requires that each of the poll registers includes a **register number field** that contains a register number of the PHY register to be polled of the PHY indicated by the address contained in the address field. In addition to Booth failing to disclose poll registers as claimed in the present invention, Booth also fails to disclose that these poll registers include a register number field. None of the cited portion of Booth describes any such register number field. Citing a large portion of text does not provide the particularity that shows which element of Booth corresponds exactly to the register number field claimed in the present invention. Claim 7 is therefore not anticipated by Booth.

Claim 8 requires each of the poll registers to include an **enable field** that enables and disables automatic polling of the PHY register to be polled. The Examiner has not established that Booth has poll registers whatsoever. Thus, the Examiner has not established that Booth discloses poll registers that include an enable field that enables and disables automatic polling of a PHY register to be polled. A review of column 14, lines 1-15 does not show any such enable field or any field remotely corresponding to such an enable field contained within a register. Switch write enable signals 506 can be generated, but these are not enable fields contained within a register. Without such an identical disclosure as that claimed, Applicant should not be denied patentability of the claimed invention.

Claim 9 requires that in one of the poll registers, the enable field is always set to enable automatic polling, the register number is set to the status register of the PHY, and the address field contains the address of a default PHY. To show each of these specifically claimed features, the Examiner merely refers to column 13, lines 35-50. As just one example of the inadequacy of the blanket references used throughout the Final Office Action in this application, Applicant hereby reproduces in its entirety column 13, lines 35-50.

> .... Instead, switching has been performed during power-up. While this simplifies the design of the network interface card, this does not provide a smooth migration path for a network user. For instance, such a design does not allow a user with an MII device (10BASE-T or 100BASE-X) to migrate to a TBI device (1000Base-X). A network interface card according to one embodiment of the present invention, however, allows such a migration path.
>
> FIG. 7—Detailed Network Interface Card Block Diagram
>
> FIG. 7 depicts a more detailed block diagram of NIC 212. FIG. 7 includes a number of elements depicted above with reference to FIG 5: PHY interface unit **412**, select generation unit **414**, link switching **420**, SERDES PHY device ...

Nowhere in this cited portion of Booth can any of the features required by claim 9 be found. Applicant is at a loss as to how column 13, lines 35-50 of Booth can be said to identically disclose any of the features of claim 9, including poll registers, an enable field always set to enable automatic polling in one of the poll registers, a register number set to the status register of the PHY, and an address field that contains the address of a default PHY. The cited portion of Booth appears to have nothing whatsoever to do with these features. These are not the particular findings required to deny patentability to an inventor based on anticipation. Accordingly, claim 9 should be considered allowable over the Booth reference.

C. The rejection of claims 11 and 12 under 35 U.S.C. § 102(e) is improper since they further define and limit a claim indicated as allowable.

In the Final Office Action, claim 10 was indicated as allowable if rewritten in independent form to include the base claims and any intervening claims. Although claim 10 has not been amended at present to be in independent form, the Examiner still deemed claim 10 as allowable over the art of record. Claim 11 directly depends from claim 10, and claim 12 depends from claim 11. Therefore, due to their dependence, claims 11 and 12 should also be considered allowable over the art of record. The rejection of these claims under 35 U.S.C. § 102(e) is therefore in error.

D. The rejection of claims 13-17 under 35 U.S.C. § 102(e) is improper since the Examiner has failed to establish that Booth identically discloses each and every element of the claimed invention.

Claim 13 relates to a method of automatically polling PHY registers of a network and comprises the steps of storing addresses of a subset of PHY registers from a plurality of PHY registers, periodically polling the PHY registers whose addresses are stored, in storing polling results obtained by the periodic polling. The polling results are compared with previous polling results and an interrupt signal is generated when the polling results are different from the previous polling results.

The Examiner, in making his rejection, does not make any specific reference to Booth regarding the storing of the addresses of a subset of PHY registers from a plurality of PHY registers. Applicant respectfully submits that this failure to particularly point out in Booth where the claimed limitation is present identically is due to Booth failing to disclose such a feature. In fact, as noted in column 19, line 57 of Booth, when the host CPU 202 begins writing a PHY, the auto polling unit 920 is able to determine the address of the PHY device that it will eventually poll. It does not state, however, that the arrangement of Booth stores addresses of a subset of PHY registers from a plurality of PHY registers. Nor does it disclose the periodic polling of the PHY registers whose addresses are stored. The Examiner has not been able to show wherein Booth the storing of addresses of PHY registers is clearly disclosed. This failure renders the rejection of claim 13 under 35 U.S.C. § 102(e) fatally flawed.

Claim 14 requires the addresses of the PHY registers to be stored in poll registers. The Examiner has not established that Booth discloses the storing of addresses of the PHY registers in poll registers. The Examiner attempted to rely upon registers 916A, and 916B as the poll registers. However, as discussed previously, these registers do not appear to be poll registers that store addresses of the PHY registers. Instead, they are disclosed in Booth as containing the status register values from

the PHY devices. Since Booth fails to disclose identically the elements of claim 14, this claim should separately be considered patentable over Booth. Claim 15 is dependent on claim 14, and should be considered allowable since it further defines and limits claim 14.

Claim 16 requires the disabling of the periodic polling by setting and clearing an enable field in the poll registers. The Examiner has failed to establish poll registers that contain an enable field. Therefore, the step of enabling and disabling periodic polling by the setting and clearing of an enable field in poll registers is clearly lacking in Booth. The rejection of claim 16 under 35 U.S.C. § 102(e) is therefore unjustified.

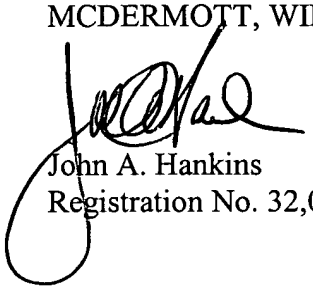
Claim 17 further requires the setting of the enable field of one of the poll registers to permanently enable periodic polling, and storing the address of a status register of a default PHY in an address field of that poll register. The Examiner attempts to support this rejection by reference to column 14, line 5-20. Applicant will not repeat this cited section of Booth, but respectfully notes that nothing in this cited section describes the setting of an enable field in a poll register, nor the permanent enablement of periodic polling, or storing the address of a status register of a default PHY in an address field of a poll register. Applicant cannot comprehend how this cited section can seriously be considered to disclose such features identically, within the intent of 35 U.S.C. § 102. Hence, claim 17 patentably defines over Booth.

XI. CONCLUSION

For the reasons advanced above, Appellant respectfully urges that the rejection of claims 1-9 and 11-17 under 35 U.S.C. § 102(e) as being anticipated by Booth, is improper. The reversal of the rejection of these claims in this Appeal is respectfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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XII. APPENDIX

1. An arrangement for polling external physical layer device (PHY) registers in a network, comprising:

a number (n) of poll registers that store information indicating which PHY registers are to be polled;

a number (m) of poll data registers that receive polled information from the PHY registers; and

poll logic that automatically polls those PHY registers indicated by the information in the poll registers as PHY registers to be polled, and stores the polled information in the PHY registers.

2. The arrangement of Claim 1, wherein the poll logic includes comparison logic that compares currently polled information with previously polled information stored in the poll data registers.

3. The arrangement of Claim 2, wherein the poll logic includes write logic responsive to the comparison logic to replace the previously polled information stored in the poll data registers with the currently polled information when the currently polled information is different than the previously polled information.

4. The arrangement of Claim 3, wherein the poll logic includes interrupt generation logic responsive to the comparison logic to generate an interrupt signal when the currently polled information is different than the previously polled information.

5. The arrangement of Claim 1, wherein n=m.

6. The arrangement of Claim 1, wherein each of the poll registers includes an address field that contains an address of a PHY containing a PHY register to be polled.

7. The arrangement of Claim 6, wherein each of the poll registers includes a register number field that contains the register number of the PHY register to be polled of the PHY indicated by the address contained in the address field.

8. The arrangement of Claim 7, wherein each of the poll registers includes an enable field that enables and disables automatic polling of the PHY register to be polled.

9. The arrangement of Claim 8, where, in one of the poll registers, the enable field is always set to enable automatic polling, the register number is set to the status register of the PHY, and the address field contains the address of a default PHY.

10. The arrangement of Claim 9, wherein each of the poll registers includes a preamble suppression field that contain information which determines whether the poll logic is to send management frames to the PHY registers without preambles.

11. The arrangement of Claim 10, wherein each of the poll registers includes a default field that contains information which determines whether the address in the address field is to be used or the address of the default PHY is to be used to determine the PHY register to be polled.

12. The arrangement of Claim 11, wherein the poll logic is configured to suppress a preamble when the default PHY accepts management frames with no preamble.

13. A method of automatically polling physical layer device (PHY) registers of a network, comprising the steps of:

storing addresses of a subset of PHY registers from a plurality of PHY registers; periodically polling the PHY registers whose addresses are stored;

storing polling results obtained by the periodically polling;

comparing the polling results with previous polling results; and

generating an interrupt signal when the polling results are different from the previous polling results.

14. The method of Claim 13, wherein the addresses of the PHY registers are stored in poll registers.

15. The method of Claim 14, wherein the polling results are stored in poll data registers.

16. The method of Claim 15, further comprising enabling and disabling the periodic polling by setting and clearing an enable field in the poll registers.

17. The method of Claim 16, further comprising setting the enable field of one of the poll registers to permanently enable periodic polling, and storing the address of a status register of a default PHY in an address field of that poll register.

18. The method of Claim 17, further comprising sending management frames without preambles to PHY registers in dependence on the setting of a preamble suppression field in the poll registers.

19. The method of Claim 18, further comprising setting a default field in the poll registers to control whether the address stored in the poll register is to be used as the address of the default PHY when a PHY register is polled.